SILICON-ON-SAPPHIRE (SOS) MONOLITHIC TRANSCEIVER MODULE COMPONENTS FOR L- AND S-BAND

D. Laighton, J. Sasonoff, J. Selin
Raytheon Equipment Division
Wayland, MA 01778

Abstract

Phase-shifter and power amplifier functional sub-assemblies have been built using monolithic circuit techniques. Silicon-on-sapphire (SOS) material is used with active devices made directly in the silicon epi layer, with lumped thin-film components used as passive elements.

Introduction

Monolithic microwave integrated circuits (MMIC's) have been designed and fabricated for use in radar applications at L-and S-bands. The design required the development of advanced silicon active devices in SOS format including MESFET devices for power amplification and insulated-gate FET (IGFET) devices for switching applications. Passive elements are fabricated simultaneously with the active devices to permit the complete fabrication of monolithic circuits.

Passive Components

Passive components including inductors and capacitors in RF MMIC's must be in lumped-element form to provide substantial size reductions. Their structure must be compatible with the fabrication process of the active devices to reduce processing complexity. Lumped-element spiral inductors and thin-film capacitors were developed using a three-layer process of aluminum, silicon dioxide, aluminum, with the silicon dioxide insulator layer forming the capacitor dielectric and providing the inductor center crossover isolation. The inductor design included computer modeling of the self-inductance of the straight sections, the mutual inductance between sections, and the ground-plane effects through the substrate.

Inductors and capacitors were fabricated to evaluate the design formulas with a range of inductor values from 0.8 nh to 9 nh, and capacitor values from 0.8 pf to 74 pf. RF losses of these lumped element components were characterized with resonant test structures consisting of a lumped-element inductor and capacitor in parallel resonance loosely coupled on the test chip by capacitive gap coupling to isolate the resonance from the generator and load. The Q values of the inductors range from 13 to about 30, depending on their size and layout dimensions.

The RF measurements of these components were made on a semi-automatic network analyzer using test fixtures and component chip designs that provided calibration down to the actual lumped-element component level. The RF calibration procedure was based on the Through-Short-Delay (TSD) method that uses calibration reference pieces that can be implemented in a form compatible with chip device interfaces.[1] The reference pieces and the components to be tested were fabricated in chip form about 3 mm square with nominal 50 ohm interfaces. A test fixture in which the chips were held with simple pressure contacts, interfaced with the network analyzer and was calibrated out of the S-parameter measurements by a de-embedding computer program that analytically removes the interconnection mismatch effects, and generates the S-parameters of the intrinsic lumped-element component.

Power Amplifier

The evolution of the 3-stage monolithic amplifier design was performed in three steps. Initially, a single-stage hybrid amplifier was designed, fabricated, and tested to show the feasibility of the SOS approach as well as to develop the necessary fabrication techniques. The next step in development was the design of a complete three-stage hybrid amplifier. The final step was a three-stage monolithic amplifier. This design approach was used to understand the layout parasitics as well as the active device characteristics and passive element values achieved as a function of the processing, before the initial design of a fully monolithic amplifier.

The three-stage hybrid amplifier was designed such that each of the three stages could be operated as an individual amplifier. Each stage includes the required DC blocking capacitors between stages, and bias networks consisting of series inductors, by-passed by fairly large value capacitors for each stage. The gate widths of three SOS/MESFET devices used were 2800 microns, 5600 microns and 12,100 microns, respectively. The actual results of this initial three-stage hybrid amplifier are shown in Figure 1. This initial hybrid investigation resulted

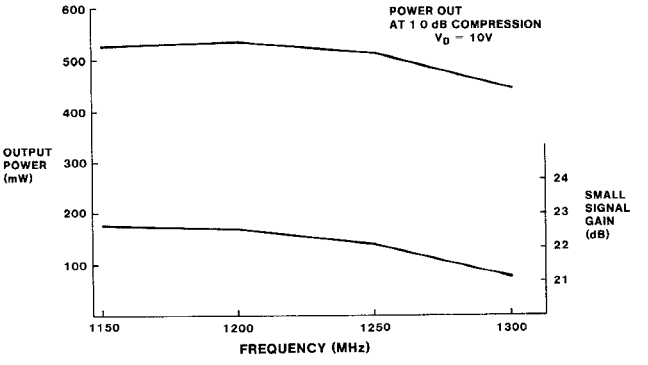

Figure 1: HYBRID POWER AMPLIFIER GAIN AND OUTPUT POWER

149-645X/81/0000-0037$00.75

in modification of the computer models to include additional parasitic effects such as the actual physical lengths of metallization connecting to ground on the circuit and measured values for dielectric thickness.

The monolithic amplifier design was based on the hybrid amplifier layout with modifications based on the differences in the parasitic effects such as lead inductances and grounding paths. In a MESFET common source amplifier, source lead inductance is the degenerative feedback mechanism and gain is generally reduced by the its presence. Source lead inductance can be minimized in the monolithic design because the source bond wires are eliminated and matching components can be grounded physically closer to the actual transistor to greatly reduce the source lead inductive parasitics. For this reason, monolithic circuits represent significant differences in characterization and computer modeling over their hybrid equivalents.

The mask layers were generated up to the first metal of the MESFET which included all of the bottom metal required for the passive elements, as well as the complete MESFET (except the source overlays). This allowed the amplifiers to be fabricated up to this point while the final circuit definition was taking place. A photograph of the completed amplifier is shown in Figure 2. The RF performance

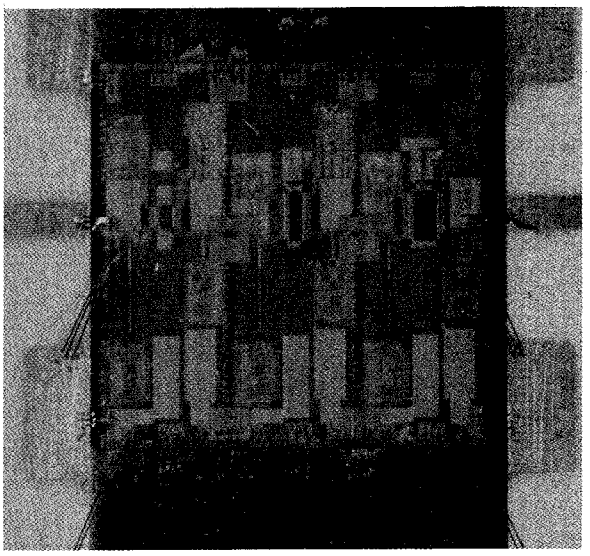

Figure 2: MONOLITHIC THREE-STAGE POWER AMPLIFIER CHIP

of the monolithic amplifier, given in Figure 3, is below that of the hybrid amplifier because of the lower drain voltage capability of the MESFET devices in these monolithic wafers.

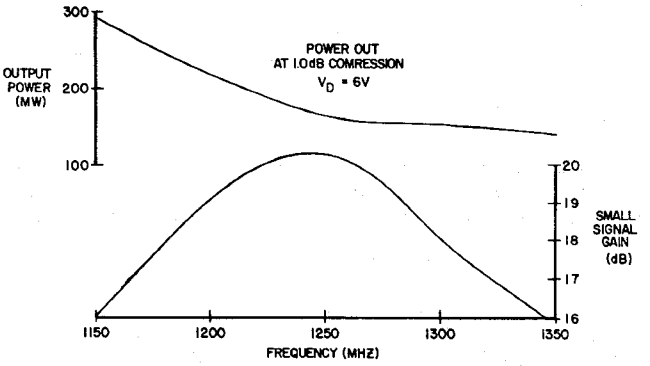

Figure 3: MONOLITHIC POWER AMPLIFIER GAIN AND OUTPUT POWER

In addition to the L-Band Amplifier, an S-Band Monolithic amplifier is also being designed. Device characterization indicated that conventional single-ended circuitry looked marginal at best for use in an S-Band power amplifier. Therefore, a push-pull integrated power amplifier concept has been utilized for the power amplifier at S-Band.

In general, SOS MESFET devices which exhibit 8 dB of gain at L-Band, roll off sharply to approximately 3 dB of gain in the S-Band frequency range. Roll off in frequency is much worse for bigger devices such as the 12,000 micron device, mostly because of the increased parasitic capacitance associated with devices with large peripheries. In order to alleviate the effects of these large parasitic capacitors it is beneficial to use two smaller devices and run these devices combined to get the power output.

The push-pull amplifier has a tremendous advantage over single-ended circuits, not only in terms of increasing the effective power output vs. frequency capability of given devices, but also because a virtual ground plane exists along the axis of symmetry of the circuit. A test configuration using two 2800 micron devices showed 5 dB gain and a 1 dB compressed output power of 247 mw at 3300 MHz.

Phase-Shifter

The phase-shifter design was implemented with insulated-gate FET (IGFET) devices used as switches. These devices are controlled by a voltage bias on the gate electrode with no current because of the insulated gate. The channel between the source and drain requires no DC bias and is modelled by a parasitic electrode capacitance in the off state of about 4 pf and by a series resistance in the on state of about 2.5 ohms. Because the only DC power dissipation required is to charge parasitic gate control lines when switching states, the IGFET device produces a phase-shifter with virtually no DC holding power required.

The phase-shifter circuit design was based on four switchable bit sections of 22.5°, 45°, 90°, and 180°, capable of providing a 360° range of phase steps. The basic phase shifter approach for all bits less than 180° is the lumped element circuit equivalent of a loaded line phase-shifter bit. A lumped element pi-section is used to synthesize the same effect as a loaded transmission line, with the capacitive loading switched by the IGFET devices. Inductors in shunt with the IGFETs are used to partially tune IGFET device capacitance to provide a flat phase shift over the frequency band.

The 180° bit uses a novel phase shifter approach. A conversion is made to a balanced transmission line system through the use of a balun and then the sense of the two sides of the balanced transmission line are switched in order to give an effective 180° phase shift. Four IGFET devices form a lumped element balun with pairs of devices switched in opposite modes, with two devices turned on and two turned off. Alternating the bias states of these pairs reverses the sense of the balun and produces a 180° phase shift.

A phase-shifter circuit was fabricated in hybrid format with separate SOS/IGFET device chips mounted on a sapphire circuit chip. The measured results of a first iteration of the phase-shifter circuit are given in Figure 4, showing the insertion phase shift for all possible phase-shift states.

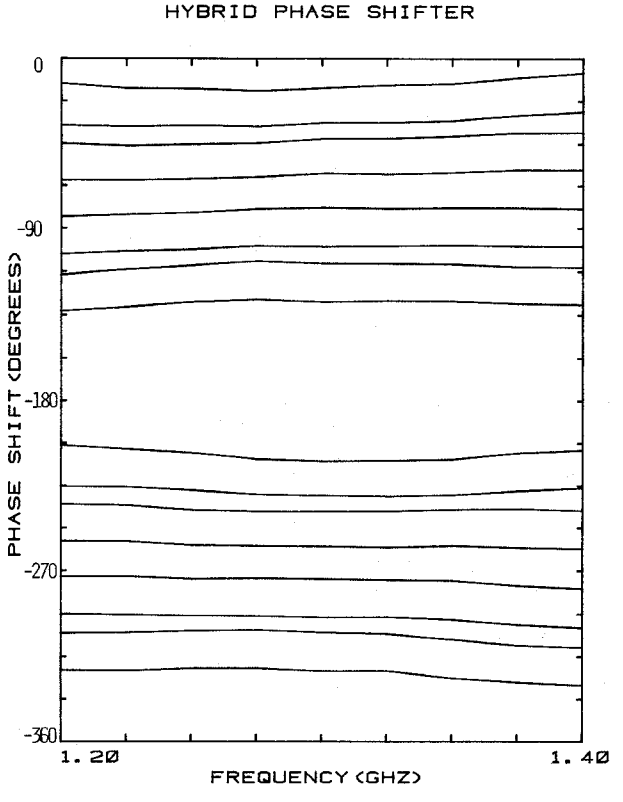

Figure 4: HYBRID PHASE SHIFTER INSERTION PHASE FOR ALL PHASE BIT COMBINATIONS

A fully monolithic phase shifter was designed and fabricated and is shown in Figure 5. Measurements of this phase-shifter showed excess phase shift steps because of layout parasitics. The circuit is presently being modified to correct the phase step errors.

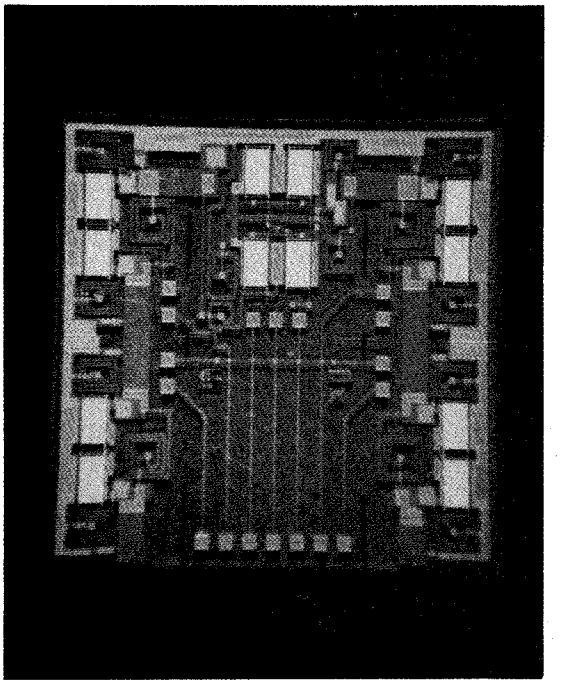

Figure 5: MONOLITHIC PHASE SHIFTER CHIP

Conclusion

Monolithic microwave integrated circuits in the form of power amplifiers and phase-shifters have been developed and show great promise of offering low-cost, lightweight radar transceiver modules.

Acknowledgement

The authors wish to acknowledge E. Lewis, A. Platzker, E. Stonebraker, and R.E. Thun, Raytheon Company, Bedford, MA for their efforts in the device design and wafer processing.

Reference

1. Speciale, R.A., "A generalization of the TSD Network-Analyzer Calibration Procedure, Covering n-Port Scattering-Parameter Measurements, Affected by Leakage Errors," IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-25 No. 12 (December 1977), pp. 1100-1115.